

Amendments to the Specification

Please add the following new section heading on page 1, line 3:

CROSS-REFERENCE TO RELATED APPLICATIONS

Please replace the paragraph beginning on page 1, line 4, and ending on page 2, line 12, with the following amended paragraph:

This patent application is related to the following co-pending U.S. Patent applications, commonly assigned and filed on August 20, 1999:

U.S. Patent Application No. 09/378,596, now U.S. Patent No. 6,853,970, entitled AUTOMATIC DESIGN OF PROCESSOR DATAPATHS, by Shail Aditya Gupta and Bantwal Ramakrishna Rau;

U.S. Patent Application No. 09/378,293, now U.S. Patent No. 6,457,173, entitled AUTOMATIC DESIGN OF VLIW INSTRUCTION FORMATS, by Shail Aditya Gupta, Bantwal Ramakrishna Rau, Richard Craig Johnson, and Michael S. Schlansker;

U.S. Patent Application No. 09/378,601, now U.S. Patent No. 6,629,312, entitled PROGRAMMATIC SYNTHESIS OF A MACHINE DESCRIPTION FOR RETARGETING A COMPILER, by Shail Aditya Gupta;

U.S. Patent Application No. 09/378,395, now U.S. Patent No. 6,385,757, entitled AUTOMATIC AUTO DESIGN OF VLIW PROCESSORS, by Shail Aditya Gupta, Bantwal Ramakrishna Rau, ~~and Vinod~~ Vinod Kumar Kathail, and Michael S. Schlansker;

U.S. Patent Application No. 09/378,298, now U.S. Patent No. 6,507,947, entitled PROGRAMMATIC SYNTHESIS OF PROCESSOR ELEMENT ARRAYS, by Robert

Schreiber, Shail Aditya Gupta, Vinod Kumar Kathail, Sadun Anik, and Bantwal Ramakrishna Rau;

U.S. Patent Application No. 09/378,397, now U.S. Patent No. 6,374,403, entitled PROGRAMMATIC METHOD FOR REDUCING COST OF CONTROL IN PARALLEL PROCESSES, by Alain Darté and Robert Schreiber;

U.S. Patent Application No. 09/378,431, now U.S. Patent No. 6,460,173, entitled FUNCTION UNIT ALLOCATION IN PROCESSOR DESIGN, by Robert Schreiber;

U.S. Patent Application No. 09/378,295, now U.S. Patent No. 6,298,471, entitled INTERCONNECT MINIMIZATION IN PROCESSOR DESIGN, by Robert Schreiber;

U.S. Patent Application No. 09/378,394, now U.S. Patent No. 6,490,716, entitled AUTOMATED DESIGN OF PROCESSOR INSTRUCTION UNITS, by Shail Aditya Gupta and Bantwal Ramakrishna Rau;

U.S. Patent Application No. 09/378,393, now U.S. Patent No. 6,438,747, entitled PROGRAMMATIC ITERATION SCHEDULING FOR PARALLEL PROCESSORS, by Robert S. Schreiber, Bantwal Ramakrishna Rau, and Alain Darté; and

U.S. Patent Application No. 09/378,290, now U.S. Patent No. 6,408,428, entitled AUTOMATED DESIGN OF PROCESSOR SYSTEMS USING FEEDBACK FROM INTERNAL MEASUREMENTS OF CANDIDATE SYSTEMS, ~~by Mike~~ by Michael S. Schlansker, Vinod Kathail, Greg Snider, Shail Aditya Gupta, Scott A. Mahlke, and Santosh G. Abraham.

The above patent applications are hereby incorporated by reference.

Please replace the paragraph beginning on page 34, line 29, and ending on page 35, line 7, with the following amended paragraph:

Each of the cache components is evaluated individually. The d-cache 1207 is evaluated as a function of cache size only, as a direct mapped cache with a line size of 16 bytes. FIG. 13 contains a Pareto curve 1301 for the d-cache 1207 for cache sizes of 2, 4, 8, and 16 kB. FIG. 13 also shows Pareto designs 1303, 1305, 1307, 1309 for the ~~d-cache 207~~ d-cache 1207. The Pareto curve 1301 is graphed with design execution time (d-cache misses N_d) on a vertical axis 1311 and cache cost (wafer area) on a horizontal axis 1313. An approximate Pareto curve 1315 connects the Pareto designs 1303, 1305, 1307, 1309.